Semi-Conductor

-> Semi-conductor are those material ~~which~~ whose conductivity lies between those of conductor & insulator.

-> Semi-conductors have forbidden energy gap of about 1ev. It behaves as a perfect insulator at about 0 kelvin. However they conduct electricity at about 0 kelvin as they have -ve coeff of resistance. For eg: Germanium & silicon

Types of semi-conductor

-> Intrinsic semi-conductor: A semi-conductor in an extremely pure form is known as intrinsic semi-conductor. No any types of impurities are doped in pure semi conductor. Thermally generated free e^-s and holes are responsible for electrical conductivity. At about 0K, they behave as insulator but as temp increases or even at room temp they conduct electricity slightly.

-> Extrinsic semi-conductor: When either pentavalent or trivalent atoms or impurities are doped to the lattice side (corner side) of pure semi conductor, extrinsic semi-conductor is formed.

-> The process of adding impurities to lattice side of pure semi-conductor is known as doping.

-> The purpose of doping is to increase no of either free e^- or holes in semi-conductor crystal to increase its electrical conductivity.

$\Rightarrow$ On the basis of doped atom. There are two types of extrinsic semi-conductor.

(i) N-type semi-conductor :- When pentavalent impurities or atoms like antimony are doped to pure germanium or silicon crystal the resulting crystal is N-type semi-conductor.
In N type semi-conductor the majority charge carriers are e⁻s whereas minority charge carriers are holes.

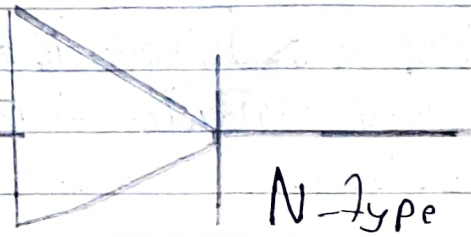
(ii) P-type semi-conductor :- When Trivalent impurities or atoms like indium are doped to pure germanium or silicon crystal the resulting crystal is P-type semiconductor.
In P type semi-conductor majority charge carrier's are holes whereas minority charge carriers are e⁻s.

P-N Junction Diode / Junction Diode / Semi-conductor diode

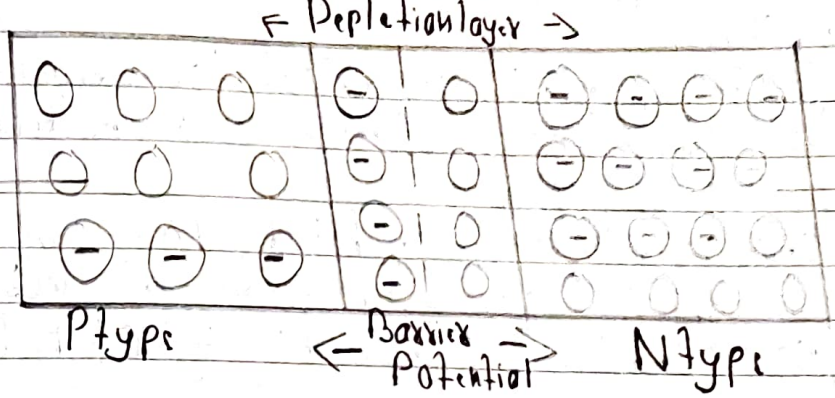
-> When P-type & N-type semi-conductor are joined together at a junction. A P-N junction is formed. However it is not formed by joining P-type semi-conductor with N-type semiconductor in Real practice.

It is formed by doping certain no of pentavalent atoms in one end of the pure semiconductor and equal no of trivalent atom in the other end of semi-conductor.

The circuital symbol of P-N junction is shown below.



Formation of P-N junction (Depletion layer & barrier potential



→ As soon as the P-N junction diode is formed there occurs the difference in concentration of charge carrier. The P region has majority of holes and minority of free electrons whereas the N-~~type~~ region has majority of free electrons and minority of holes. Due to the difference in concentration of charge carrier ~~their~~ there occurs the diffusion of holes from P to N-region and free electrons from N-region to P-regi

During the process, free e⁻ & holes recombine near the junct Due to recombination the region near the junction is dep ted (emptied) of free electrons & holes which is kn as depletion layer or depletion region. Its width i about 10^{-3} cm to 10^{-6} cm

During the process of diffusion +ve ion is create beside the junction in N-region & -ve ion is cre beside the junction in P-region. After sometime wall of +ve ion & -ve ion is created beside t junction which further prevents diffusion of cha carries. Thus, a potential difference called barrier tial is set across the junction.

→ Its value depends on the nature of crystal, temp^{r} & amount of doping.

→ The value of barrier potential for germanium is 0.3V & that for silicon is 0.7V at room temp^{r}.

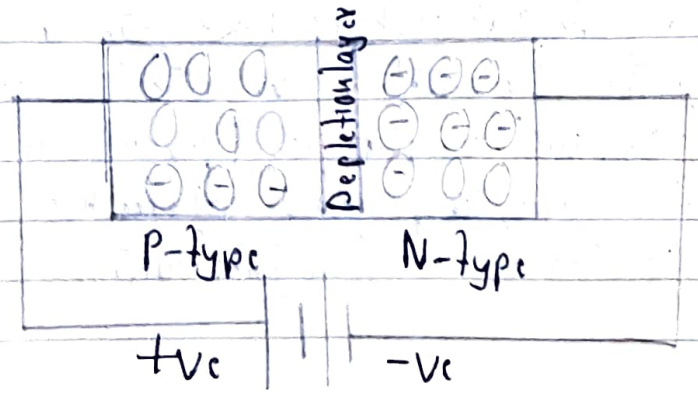
Biasing of P-N Junction Diode: Process of connecting the external voltage source (battery) across the P-N junction diode is known as biasing of P-N Junction Diode.

A P-N Junction Diode can be biased in two diff ways.

(I) Forward Biasing: A PN Junction Diode is said to be forward biased if its P-side is connected to +ve terminal of external voltage source (battery) & N-side is connected to -ve terminal of external voltage source.

The characteristics seen during forward biasing of P-N Junction Diode is given below:

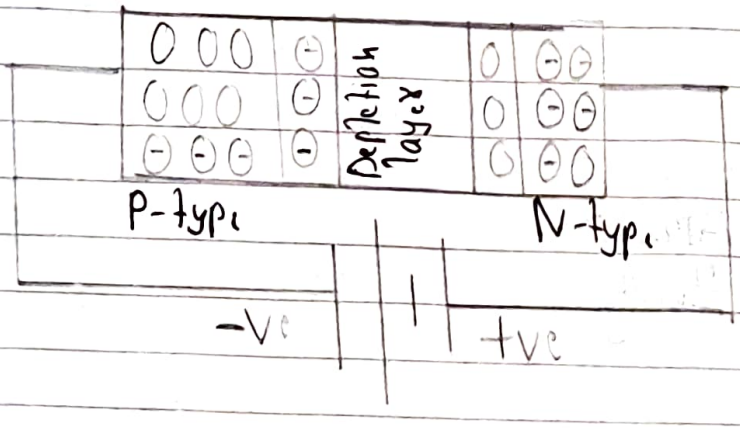
(i) The width of depletion layer decreases.
(ii) Barrier Potential decreases
(iii) Flow of current inside P-N Junction diode is due to flow of majority charge carrier.
(v) During forward biasing, diode offers very low resistance known as forward resistance.



(2) Reverse Biasing: A P-N junction diode is said to be reverse biased if its P-side is connected to -ve terminal of external voltage source & N-side is connected to +ve terminal of emf voltage source.

* Characteristics seen during reverse biasing of P-N junction diode is:

(1) Width of depletion layer increases
(2) Barrier Potential increases
(3) Flow of negligable or zero current inside P-N junction diode is due to flow of minority charge carrier.
(4) During reverse biasing diode offers high resistance called reverse resistance & behave as a open switch.



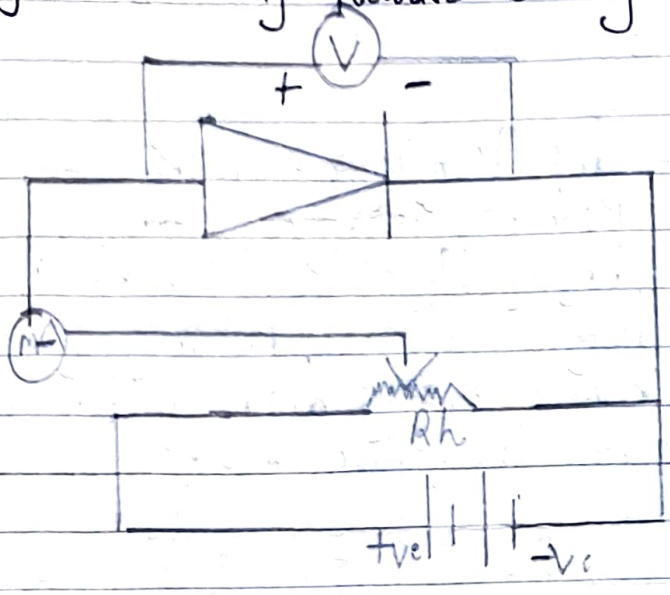
* Insulators have forbidden energy gap of >3 where as conductors are overlapped

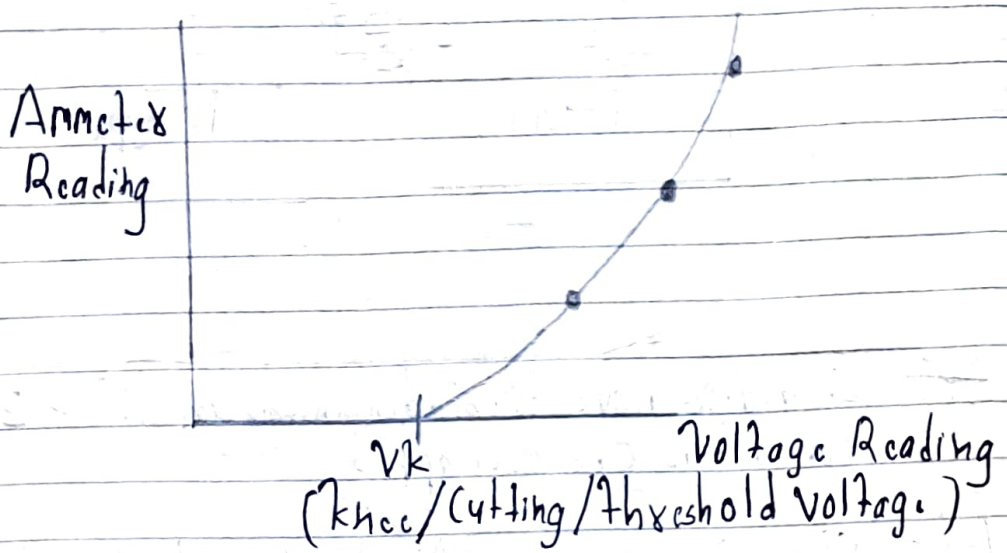
Characteristics of PN-Junction diode (V-I graph)

→ The graph between the voltage across the junction diode & current through it is called characteristics of junction diode. There are two types of diode characteristics.

(1) Forward Characteristics of PN Junction diode: It is the graph showing the variation of circuit current with forward biasing voltage.

The arrangement for studying characteristics curve of a PN junction during forward biasing is shown below.





The above characteristics can be studied by changing circuit resistance with the help of rheostate so that voltage across the diode changes & hence current through it. For diff value of voltage, the value of current is noted & the nature of graph of V & I is shown above. This V-I current graph is called forward characteristics.

Following obs are made by studying the graph.

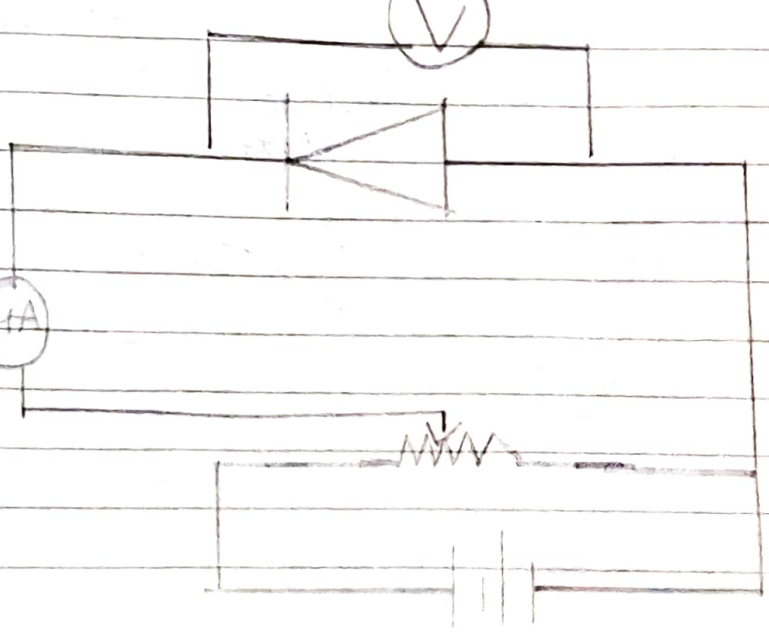
(i) The voltage current isn't a st line, i.e Junction diode does not obey Ohm's law.

(ii) Initially the current increases slowly, till the voltage across the diode crosses a certain value called knee voltage (V_k) before this voltage depletion on layer plays a dominant role in controlling the motion of charge carrier.

(iii) After knee voltage, the diode current increases rapidly even for a very small increase in voltage across the diode. Here, the Majority charge carrier fills very small resistance at the junction.

(2) Reverse characterstics of PN Junction diode: It is the graph showing the variation of circuit current with reverse biasing voltage. The exp arrangement for studying the characteristics for a PN junction diode during the reverse biasing is shown below. Here a micro ammeter is used to measure current with the reverse bias voltage.

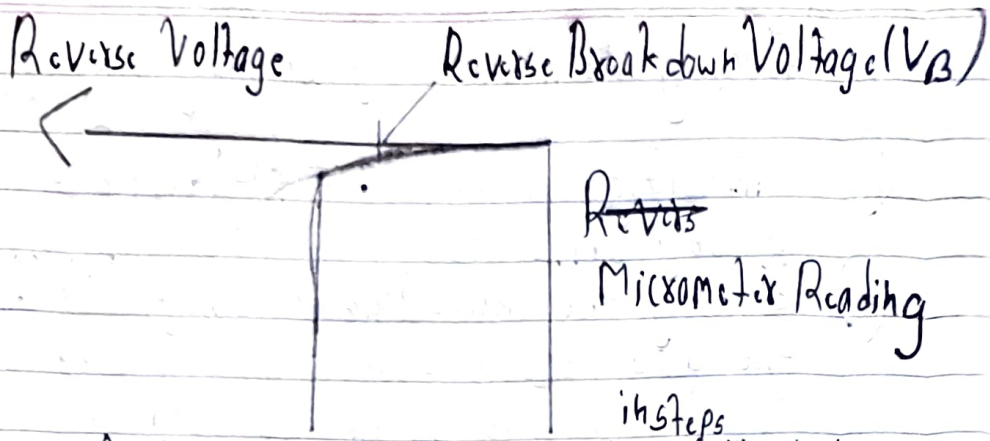
A VI graph is obtained which is called reverse characteristics of PN junction diode.



PN junction operate in forward bias

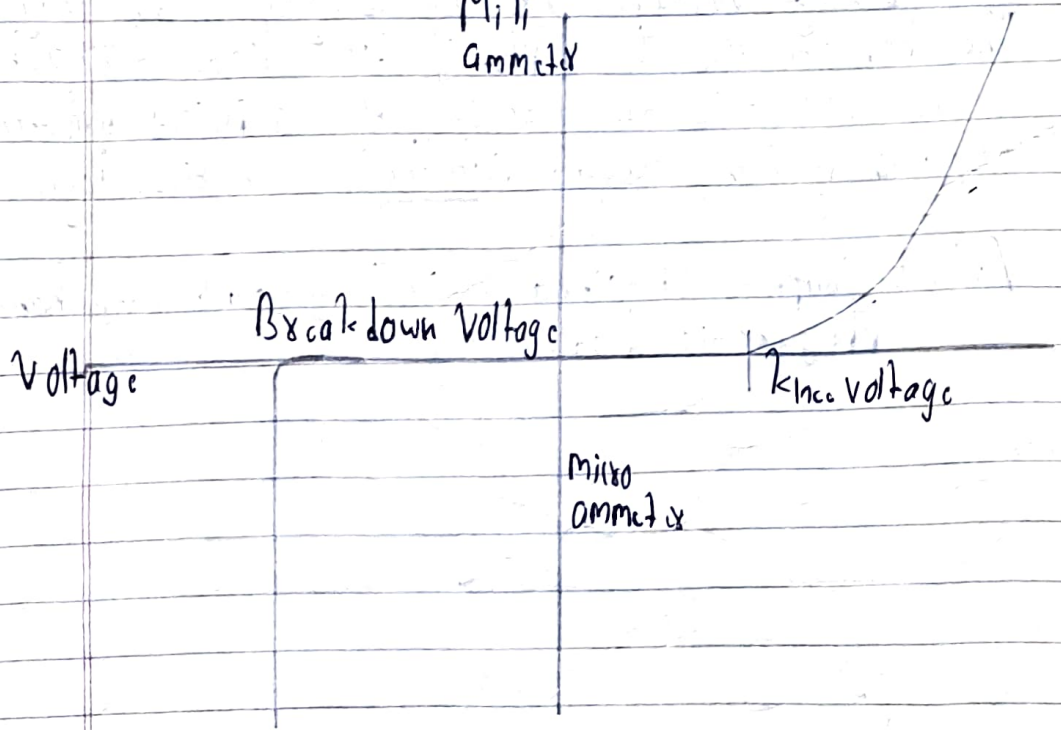
Heavy dope / Break down → because of Zener effect

light dope → avalanche effect



The reverse voltage is slowly increased with the help of rheostat. & corresponding μA (microammeter) reading is noted. with the reverse bias voltage the current remains very small over a long range, with the increasing reverse voltage. (increasing slightly) Once the external voltage exceeds a particular voltage the current increases rapidly.

The reverse voltage beyond which the diode current increases rapidly is known as reverse breakdown voltage.



Imp → Reverse voltage में current conduct होता है
Why (uA)? → क्योंकि उसमें minority charge carrier

Zener Effect :- A zener effect is a type of reverse breakdown that occur in heavily dopped PN junction diode typically at low reverse voltage (less than 5V).

Avalance Effect :- A avalance effect is a type of reverse breakdown in a diode that occur in lightly dopped PN junction diode in higher reverse voltage (greater than 6V)

Q. Diff bet^wn Zener & Avalance breakdown.

	Zener breakdown	Avalance breakdown
(i)	It occurs in heavily dopped diode.	It occurs in lightly dopped diode.
(ii)	It occur at low reverse bias voltage.	It occur at high reverse bias voltage
(iii)	Strong electric field is produced at a junction.	Weak electric field is produced at a junction.
(iv)	Thin depletion layer is seen	Thick depletion layer is seen

Zener diode :- A special type of diode designed to conduct in reverse ⇒ when the voltage across it reaches a specific value called Zener breakdown voltage.

Symbol

Zener Diode.

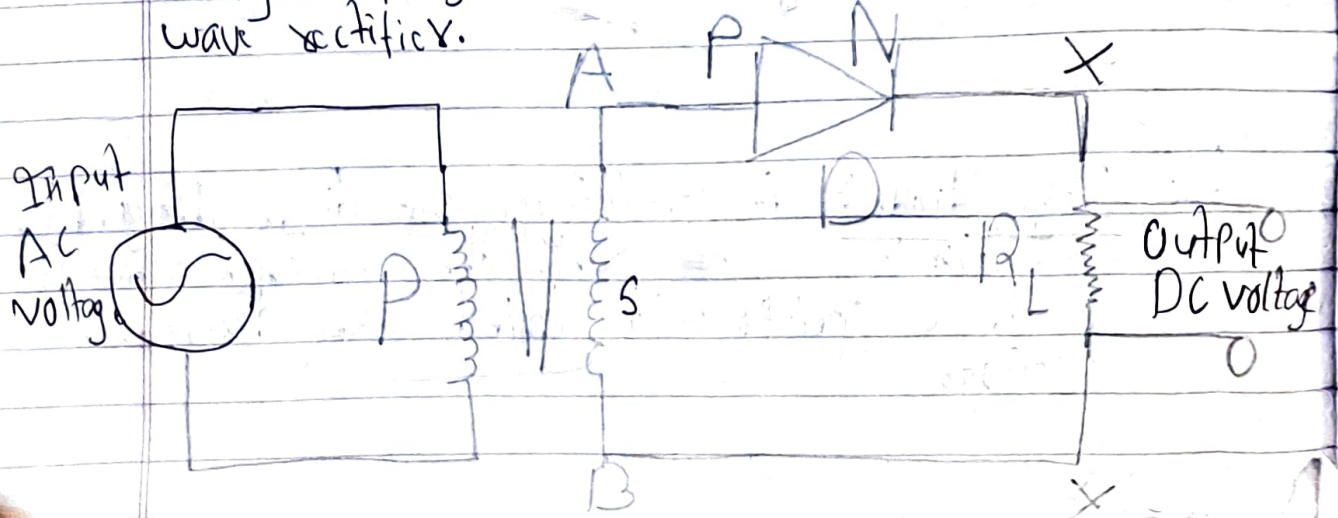
Rectifier:- The process of conversion of AC into DC is called rectification & the device used for this purpose is called rectifier.

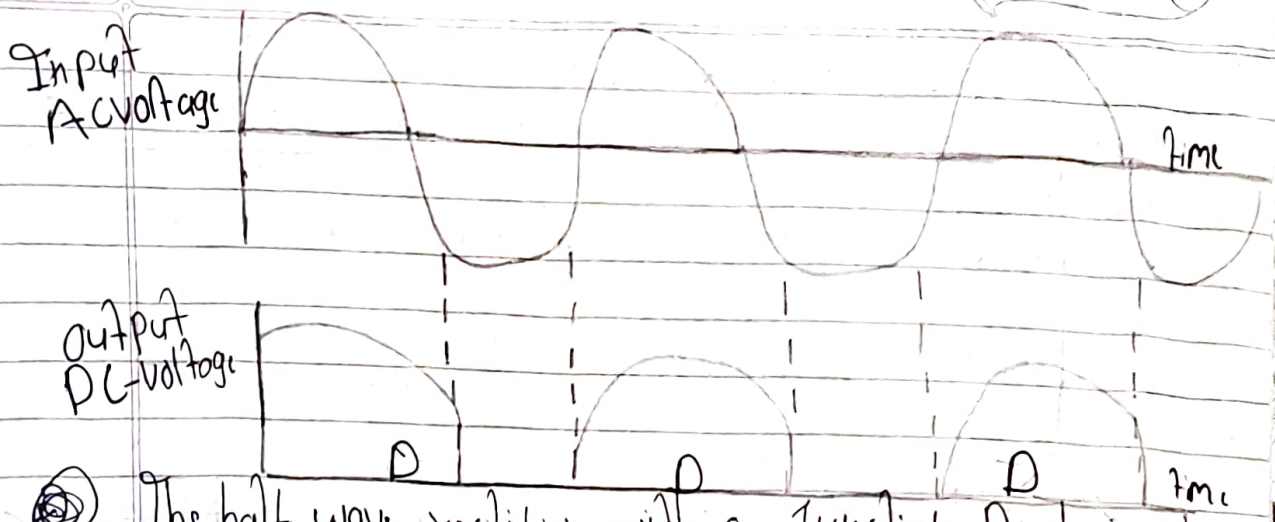
Principle of Rectifier:

When a PN junction diode is forward biased it offers low resistance & the current flow through it but when it is reverse biased it offers high resistance & almost no current flow through it. This unidirectional property of the diode enable it to be used as rectifier. There are two types of rectifier.

(1) Half wave rectifier (2) Full wave rectifier.

(1) Half wave rectifier: The rectifier which converts only half cycle of AC into DC is called half wave rectifier.





The half wave rectifier with a Junction Diode is shown above in the figure. The input voltage is supplied in the primary coil of the transformer. The secondary coil of the transformer is connected to PN Junction Diode D & load resistance as shown above in the fig.

During the +ve half cycle of AC, let us say the end A of secondary coil of transformer is +ve while the end B is negative. The Diode is forward biased & hence the current flow through the Diode & seen across the load resistance (R_L) from X to Y.

During the -ve half cycle of AC, the end A of secondary coil of transformer is -ve while the end B is +ve. The Diode is reverse biased & hence no current is seen across the R_L.

Hence, the half cycle of AC is converted into DC across the load resistance

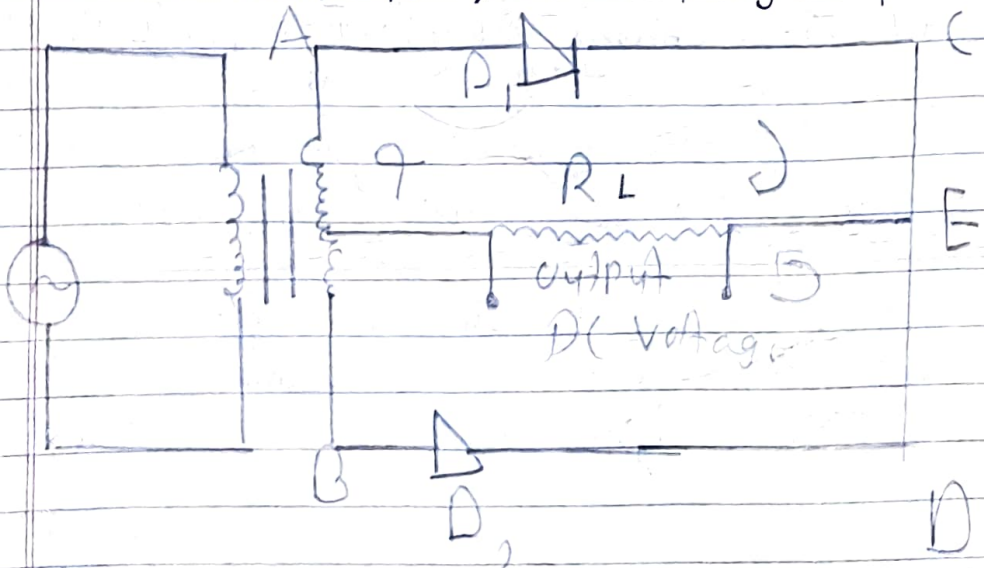
(2) Full Wave Rectifier: The rectifier which converts both +ve & -ve half cycle of AC into DC is called Full wave rectifier.
There are two types of full wave rectifier.

(1) Central tapped full wave Rectifier
(2) Bridge Rectifier

(1) Full wav. ~~The rectifier which convert both +ve & -ve half cycle of AC to DC is called full wave rectifier.~~

There

(1) Central tapped rectifier is the full wave rectifier that convert both +ve & -ve half cycle of AC into DC.



Graph sample

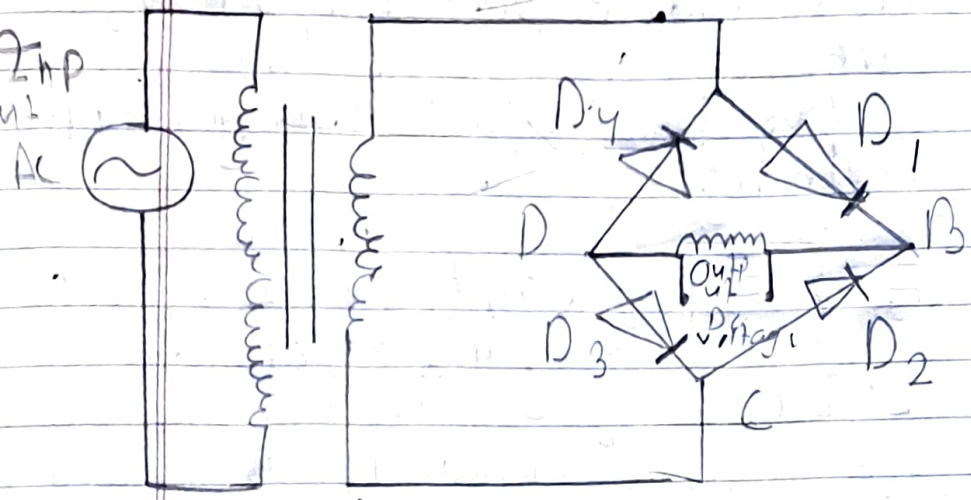
The input AC voltage in the primary coil of the transformer. The ends of secondary coil of the transformer are connected with P-side of two P-N junction diode. The N-side of the both the diodes are connected with load Resistance which is centrally tapped as showed in the fig.

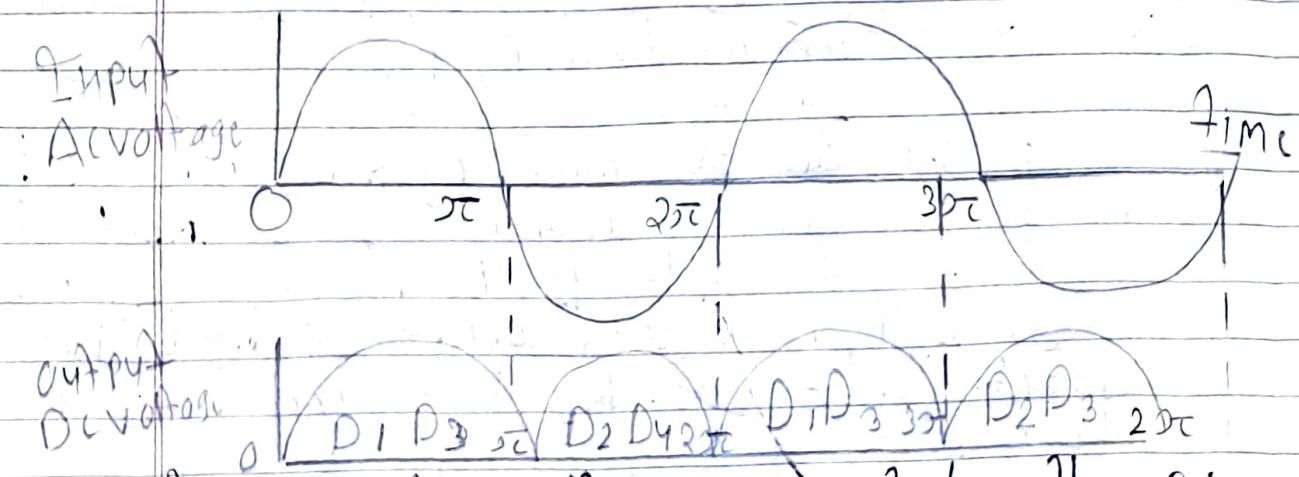
During the +ve half cycle of AC, let us say the end 'A' of sec coil of the transformer becomes +ve while the end 'B' becomes negative. The diode D_1 is forward biased whereas Diode D_2 is reverse biased. Diode D_2 doesn't conduct current across load resistance is thru the diode D_1 from E to F.

During the -ve half cycle of AC, the end B of sec coil of transformer becomes negative, while the end B becomes +ve. D_2 is forward & D_1 is reversed biased Diode D_1 doesn't conduct. Current across R_L is thru the Diode D_2 from E to F.

Hence: both the cycle of AC is converted to DC.

(B) Bridge rectifier is a full wave rectifier which converts both +ve & -ve half cycle into DC





The input AC voltage is supplied in the primary coil of the transformer. The ends of the secondary coil of the transformer is connected with 4 PN junction diode & load resistance as shown in the figure. Diodes are arranged in such a way that two diodes are forward bias during +ve half cycle of AC & remaining two diodes are forward bias in -ve half cycle of AC.

During the +ve half cycle of AC, let us say the end x of secondary coil of transformer is +ve while the end y. The diode D_1 & D_3 are

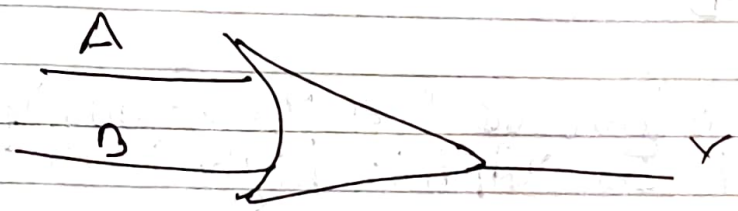
forward biased while diodes D_2 & D_4 are reverse bias. The diode D_2 & D_4 doesn't conduct. Current across the load resistance thru the diode D_1 & D_2 from B to D.

During -ve half cycle of AC, ~~the end A of sec coil of transformer~~ from let us say the end (X) of secondary coil of transformer is +ve & 'x' is -ve. The diode D_2 & D_4 are forward biased while Diode D_1 & D_3 are reversed biased. D_1 & D_3 don't conduct. Current across R, thru D_2 & D_4 from B to D.

Logic gate: Are the electronic circuit that gives the logical decision. The function of logic gate are based on the Boolean alg. There are two types of logic gate.

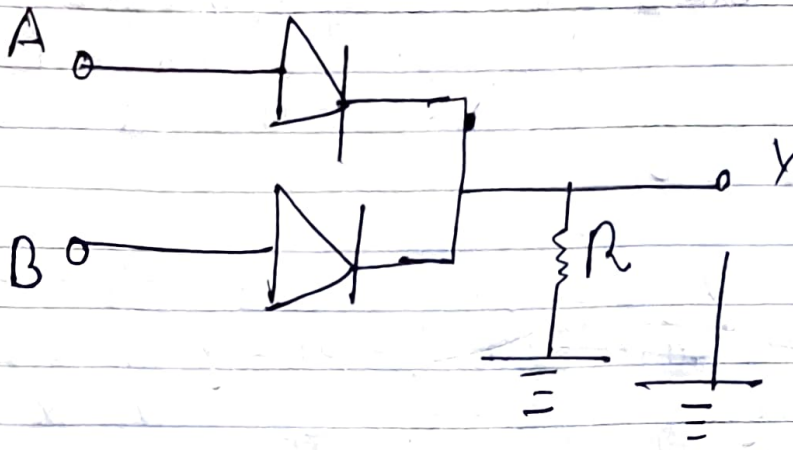
1. Simple logic gate : OR, AND, OR, ~~NOR, OR, NOR~~
2. Compound logic gate

1. OR gate: It has two or more than two input & single output. It's output is high if any or all inputs are high.



Boolean Alg: Y = A+B

A	B	Y
0	0	0
1	0	1
0	1	1



OR gate using diode

(1) When A = 0 & B = 0 both are reverse-biased & donot conduct. So output Y = 0

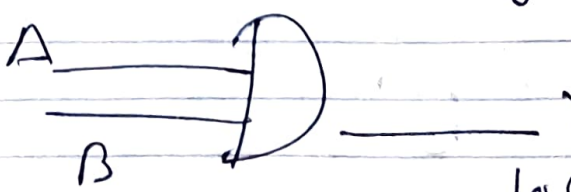
(2) When A = 1 & B = 0, diode D_1 is forward biased & conduct while diode D_2 is reverse biased & donot conduct. So, output Y = 1

(3) When A = 0 & B = 1 diode D_1 is reverse biased & donot conduct while the diode D_2 is forward biased & conduct so output Y = 1

(4) When A = 1 & B = 1 both are forward biased & conduct so, output Y = 1.

(2) AND

→ It has two or more than two input & single output. Its output is high if all the inputs are high.

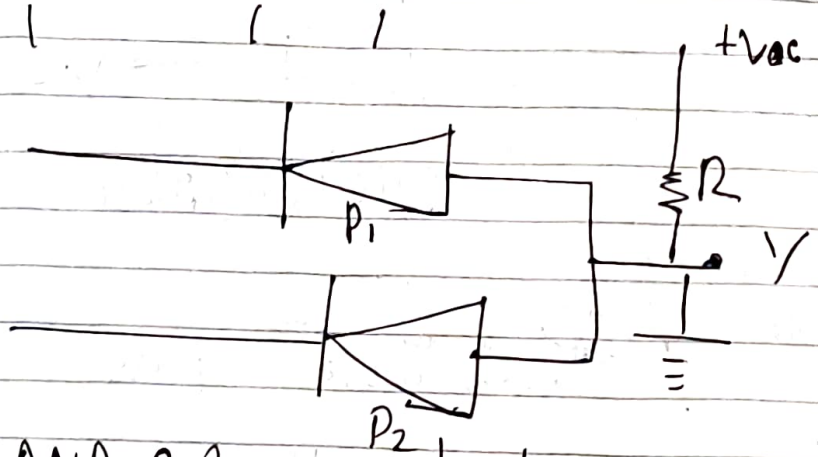


logical symbol

Boolean Algebra : $Y = A \cdot B$

Truth table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



AND Gate using diodes

(1) When A = 0 & B = 0 both the diodes are forward biased but shorted (certain) so output Y = 0

(2) When A = 1 & B = 0 diode D_1 is reverse-biased & do not conduct while diode D_2 is forward biased & shorted so output Y = 0

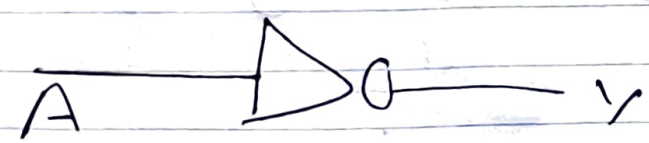
(3) When A = 0 & B = 1 diode D_1 is forward biased & shorted while d_2 is reverse biased & do not conduct So, output Y = 0

(4) When A = 1 & B = 1 both diode D_1 & D_2 are reverse biased & do not conduct output Y = 1 due to external voltage source

Transistor

(3) NOT gate

It has single input & single output. It's output is high if the input is low.



logical symbol

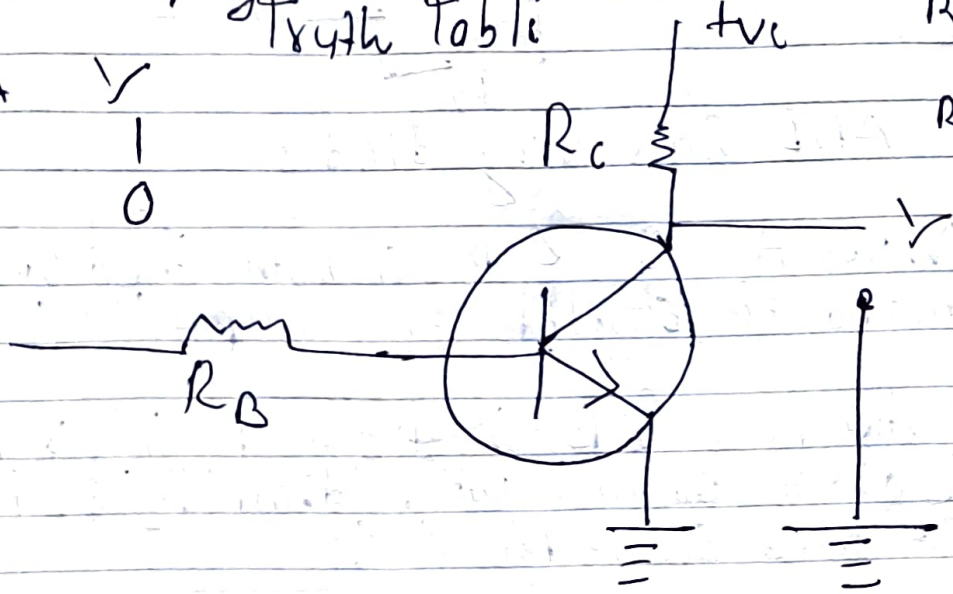
Boolean Algebra: $Y = A'$

Truth Table

A	Y
0	1
1	0

R_B -> Resistor with base

R_C -> with collector



NOT gate using transistor

Compound logic gate

Compound logic gate are formed by combination of two or more basic logic gate.

(i) NOR gate :- It has two or more inputs & single output which output of OR gate is connected to not gate & its output is high if all inputs are low.

Boolean Algebra $Y = \overline{A+B}$

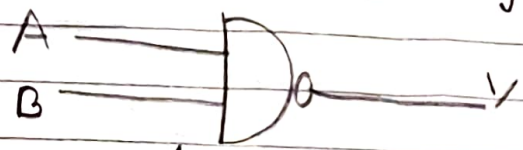
Logical symbol :- NOR gate

Truth Table :-

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

(ii) NAND gate :- It has two or more inputs & single output. when output of AND is connected as input of NOT gate, NAND gate is formed. Its output is high if any or all inputs are low.

Boolean Algebra :- $Y = \overline{A \cdot B}$



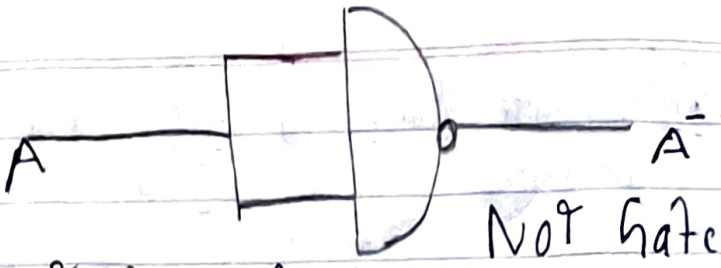
Logical Symbol

Truth Table :-

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NAND gate as universal gate.

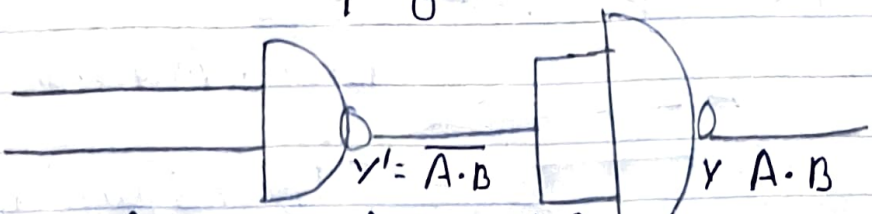
-> NAND gate is univers al gate because its repeated use can produce other logic gate.



Not Gate from NAND

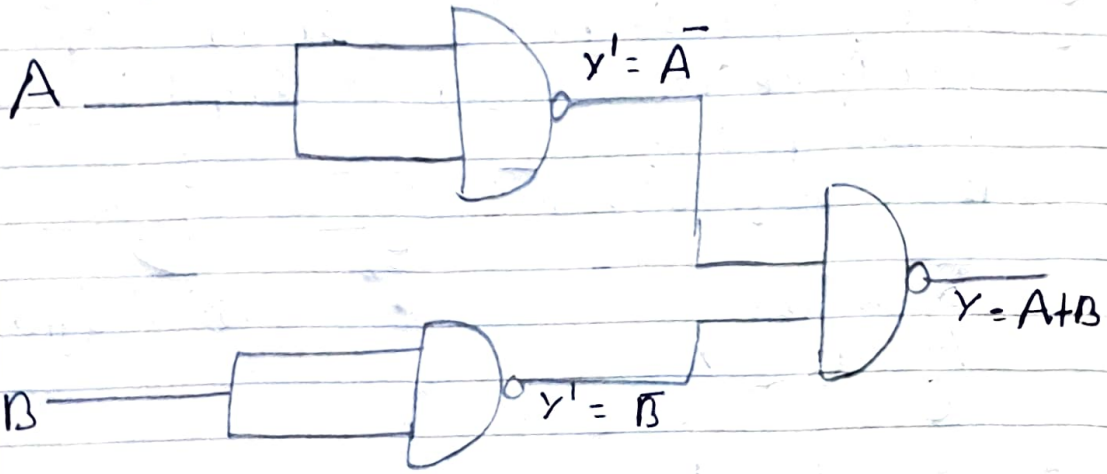
Truth Table

A	Y
0	1
1	0



AND Gate from NAND Gate

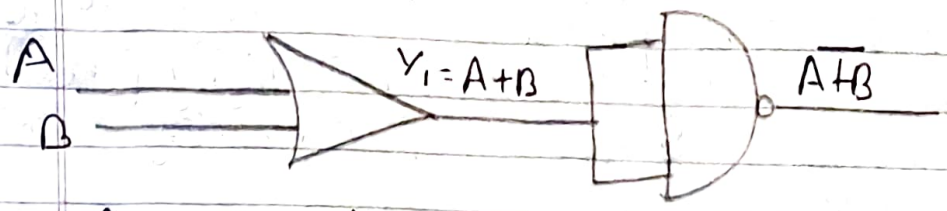
A	B	Y'	Y
0	0	1	0
1	0	1	0
0	1	1	0
1	1	0	1



OR Gate from NAND Gate

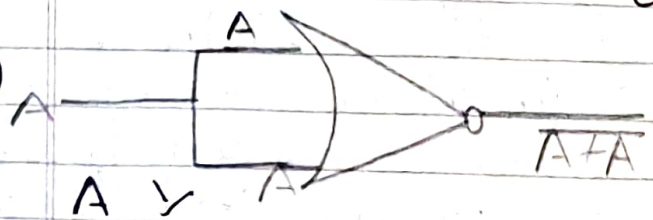
A	B	$Y' = \bar{A}$	$Y' = \bar{B}$	Y
0	0	1	1	0
1	0	0	1	1
0	1	1	0	1
1	1	0	0	1

Q. For the digital circuit given below, write the truth table showing output for all possible input A, B & identify gates obtained from the combination.



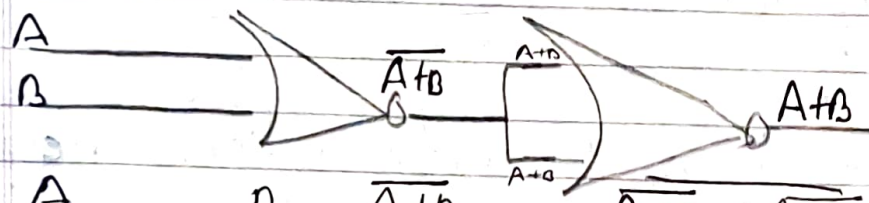
A	B	$Y_1 = A+B$	Y
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

(i)



A	Y
0	1
1	0

(ii)

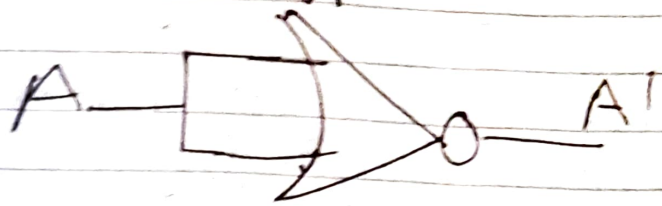


A	B	$\overline{A+B}$	$\overline{A+B} + \overline{A+B}$
0	1	0	1
1	0	0	1
0	0	1	0
1	1	0	1

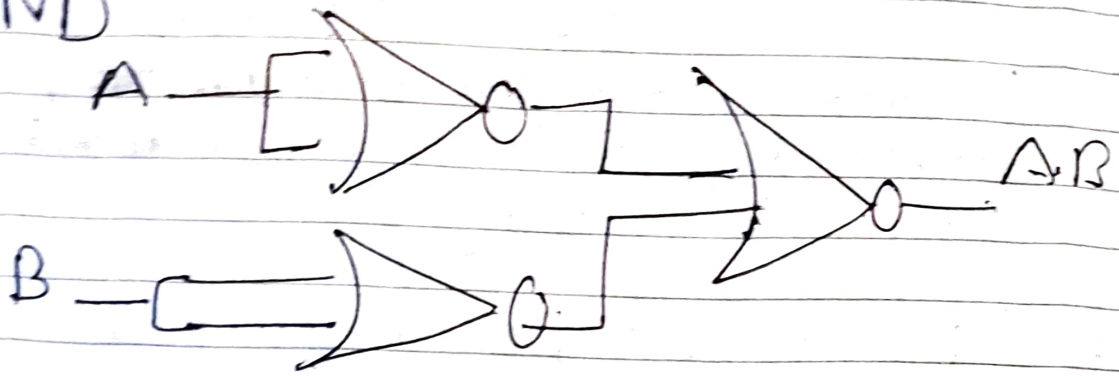
$\overline{A+B} + \overline{A+B}$

$0+0=0$
$0+0=0$
$1+1=1$
$0+0=0$

NOT from NOR



AND



OR